REMARKS

Reconsideration and allowance of the subject application in view of the foregoing amendments and the following remarks is respectfully requested.

Applicants appreciates the courtesies shown to Applicants' representatives by Examiner Diaz in the March 31, 2009 personal interview.

In response to the rejection of claims 1-6 under 35 U.S.C. §103(a) over Riseman (US 4,169,000) in combination with Applicants' Admitted Prior Art (AAPA), and based upon the Examiner's helpful comments presented during the personal interview, claims 1-6 are amended and, as presented below, are believed to be patentable over the applied art.

As amended, claim 1 recites, *inter alia*, a semiconductor device comprising "a buffer layer having a plurality of spaced apart shapes formed on, and extending above, a planar upper surface of a lower substrate." The upper substrate is adhesively attached to the spaced apart shapes and because of the space between the shapes, the reduced surface area that forms the adhesive surface permits the upper substrate to be easily removed from the lower substrate. The applied references fail to disclose, teach, or suggest this feature.

The abstract of Riseman discloses a "method for forming a fully-enclosed air isolation structure which comprises etching a pattern of cavities extending from one surface of a silicon substrate into the substrate to laterally surround and electrically isolate said plurality of substrate pockets." As a result of the etching, the unetched material forms isolated islands of substrate, and cannot be characterized as part of a

buffer layer having a plurality of spaced apart shapes formed on a planar upper surface of a lower substrate.

In other words, unlike amended claim 1, wherein a buffer layer is formed on top of a planar surface, Riseman forms enclosed air gaps by etching into the substrate. The resulting upper surface of the substrate is not planar, as recited in claim 1.

Still further, Applicants' respectfully submit that base upon the buffer layer with spaced apart shapes being formed on a planar lower substrate, the buffer layer is open on the lateral edges of the substrate and are therefore the space formed between the shapes are neither cavities in the substrate nor are they fully enclosed. This feature is distinguished from Riseman's fully enclosed cavity patterns, (*see* Figs 5-7 and column 6, lines 9-13). According, the Applicants' claimed buffer layer with spaced apart shapes is distinguished from Riseman's enclosed and isolated cavities etched in the substrate.

Furthermore, Applicants respectfully submit that the alleged combination of references not only fails to disclose, teach or suggest all of Applicants' recited claim features, but in addition, the alleged combination of references is improper because one of ordinary skill in the art would not be motivated to combine Riseman's method of forming an integrated circuit structure with fully-enclosed air isolation cavities with AAPA.

Applicants respectfully submit that neither Riseman nor AAPA suggest the desirability of combining such teachings and therefore, the Office Action appears to use improper hindsight reconstruction to pick and choose among isolated disclosures. Although Riseman suggest that the cavities reduce stress induced by changes in volume, Applicants respectfully submit that one or ordinary skill in the art would not be motivated

to combine etched cavities in the substrate, formed primarily for their dielectric properties, with the AAPA to render obvious the Applicants' recited structure. Accordingly, it is respectfully submitted that the combination is improper.

Furthermore, even if combined, the combination would result in etching the AAPA's lower substrate 1 to form enclosed cavities and would not render obvious buffer shapes formed on and extending from the lower substrate, as recited in amended claim 1.

Applicants respectfully submit that as amended, independent claim 1 is patentable not only due to the failure of Riseman in view of AAPA to disclose, teach or motivate all recited features of the claims, but is also patentable based upon the improper combination of the applied references.

Claims 2-6 depend from independent claim 1 and are likewise patentable over the asserted combination of references for at least their dependence on an allowable base claim, as well as for the additional features they recite. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the present application should be in condition for allowance and a Notice to that effect is earnestly solicited.

The Examiner is invited to telephone the undersigned, Applicants' attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,
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